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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,406	02/12/2001	S. Brandon Keller	10007975-1	1870

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EXAMINER	
ROSALES HANNER, MORELLA I	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/782,406	KELLER ET AL.	
	Examiner	Art Unit	
	Morella I Rosales-Hanner	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. **Claims 1 – 20** have been examined and are pending.

Information Disclosure Statement

2. The office acknowledges receive of the information disclosure statement (IDS) submitted on February 5th 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3.1 **Claims 1 – 5, 7 – 13, 15 –18 and 20** are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **U.S. Patent No. 6,292,582 issued to Lin et al.**, hereafter referred to as *Lin*.

3.1.1 As regard to **claim 1**, *Lin* teaches **[Fig 2 and corresponding text]** an integrated defect (which includes violations to specification) detection, classification, diagnosis and repair system, the method comprising:

- reading defect records (violations of a specification) for a circuit design **[Col 22, lines 62 - 67]**;
- diagnosing the defects (identifying symptoms of the violations) based on the circuit design **[Col. 7, lines 22 – 42]**;
- generating a precise image of the repair (identifying solutions to the violations) based on the symptoms, using data stored in a repair knowledgebase (solutions database) **[Fig 26 and corresponding text]**; and
- proposing a repair (solution) based on data stored in a (knowledgebase) **[Fig. 26 and corresponding text]**.

3.1.2 As regard to **claim 2**, *Lin* teaches **[Col 8,lines 1 - 19]** a method for analyzing a circuit design, further comprising:

- running a design tool on the circuit design; and
- detecting defects (violations of the specification) using a CAD tool.

3.1.3 As regard to **claim 3**, *Lin* teaches [**Col. 22, lines 62 - 67**] a method for analyzing a circuit, further comprising storing the defects (violations) into a file, and wherein the step of reading defects comprises reading the defects file.

3.1.4 As regard to **claim 4**, *Lin* teaches [**Col 31, lines 46 - 51**] a method for analyzing a circuit design further comprising configuring the CAD tool to the circuit design using a configuration file.

3.1.5 As regard to **claims 5, 12 and 17**, *Lin* teaches [**Section IV. Automated Defect Repair**] a method for analyzing a circuit design further comprising:

- receiving a selected repair (solution);
- re-configuring a CAD tool based on the repair; and
- re-running the CAD tool on the design.

3.1.6 As regard to **claim 7**, *Lin* teaches [**Col 22, lines 62 - 67**] editing a configuration file of the CAD tool.

3.1.7 As regard to **claim 8**, *Lin* teaches [**Section VI. Knowledgebase Generation, Management and Optimization**] storing data related to diagnosis (symptoms) and repairs (solutions) for the circuit in the knowledgebase (solutions database).

3.1.8 As regard to **claim 9**, *ref* teaches **[Figs. 1, 2 and 26 and corresponding text]** the steps of reading defects (violations), diagnosing (identifying symptoms), identifying repairs (solutions), and proposing the proposed repair (solution) comprise using a software configuration tool stored in a computer memory.

3.1.9 As regard to **claim 10**, *Lin* teaches **[Figs 1 & 2 and corresponding text]** a computer system for **analyzing signals** in a circuit design stored in a memory, the system comprising:

- a storage medium; **and**
- a processor for executing a software program stored on the storage medium for analyzing a circuit design, the software comprising a set of instructions for:
    - reading defects (such as violations of a specification) for a circuit design **[Col 22, lines 62 - 67]**;
    - diagnosing the defect (identifying symptoms of the violations) based on the circuit design **[Col 7, lines 22 - 42]**;
    - identifying repairs to the defects (solutions to the violations) based on the diagnosis (symptoms), using data in a knowledgebase (solutions database) **[Fig 26 and corresponding text]**; **and**
    - proposing a proposed repair (solution) based on data stored in the knowledgebase (solutions database) **[Fig 26 and corresponding text]**.

3.1.12 As regard to **claims 11 and 16**, *Lin* teaches **[location]** a method further comprising:

- configuring an E-CAD tool to the circuit design using a configuration file [**Col 31, lines 46 - 51**];
- running the E-CAD tool on the circuit design [**Fig 26 and corresponding text**];
- detecting violations of the specification using the E-CAD tool [**Col 8, lines 1 - 19**]; and
- storing the violations to a violations file [**Col 22, lines 62 - 67**]; and
- reading violations from a violations file [**Col 22, lines 62 - 67**].

3.1.10 As regard to **claim 13**, *Lin* teaches [**Fig 26 and corresponding text**] a system further comprising instructions for:

- receiving a selected repair (solution); and
- editing a configuration file of a CAD tool based on the selected repair (solution).

3.1.11 As regard to **claim 15**, *Lin* teaches [**Fig 2 and corresponding text**] a computer-readable medium having computer-executable instructions for performing a method for a representation of a circuit design, the method comprising:

- reading defects (such as violations of a specification) for a circuit design [**Col 22, lines 62 -67**];
- diagnosing (identifying symptoms) of the violations based on the circuit design [**Col 7, lines 22 - 42**];
- generating a precise image of a repair (identifying solutions to the defects) based on the symptoms, using data in a solutions database [**Fig 26 and corresponding text**]; and

- proposing a proposed solution based on data stored in the solutions database

[Fig 26 and corresponding text].

3.1.12 As regard to **claim 18**, *Lin* teaches **[Fig 26 and corresponding text]** a method further comprising:

- receiving a selected solution; and
- editing a configuration file of an E-CAD tool based on the selected solution.

3.1.13 As regard to **claim 20**, *Lin* teaches **[Fig 26 and corresponding text]** a method further comprising re-running the E-CAD tool on the circuit design.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4.1 Claims **6, 14 and 19** rejected under 35 U.S.C. 103(a) as being unpatentable over *Lin,* as applied to claims 1 – 5, 7 –13, 15 –18 and 19 above, and further in view of **U.S. Patent No. 6,553,548 issued to Hekmatpour**, hereafter referred to as *Hekmatpour.*

4.1.1 As regard to **claims 6, 14 and 19**, *Lin* teaches **[Fig 26 and corresponding text]** a method of identifying repairs (solutions).

Lin does not expressly teach method of where a repair (solution) is identified and it is proposed by displaying it on a display device, and receiving an input signal from an input device.

Hekmatpour teaches **[Design Error Recovery section]** a system and method for recovering from design error in an integrated circuit design environment that involves user interaction.

Hekmatpour also teaches **[Col 3, 2nd full paragraph]** that identification of design errors as early in the design process as possible is important in order to minimize the cost of redesign.

It would have been obvious to one of ordinary skills in the art to modify the method and system for identifying repairs (solutions) in an integrated circuit design

environment as disclosed by Lin to interact with a user during design error recovery in order to minimize the cost of circuit redesign as taught by *Hekmatpour*

Additional references

5. The following is a list of references that are relevant to the claimed invention but were not cited by the examiner:

- Nagaraj NS, Poras Balsara and Cyrus Cantrell, "Bridging the gap between TCAD and ECAD Methodologies in Deep Sub-micron Interconnect Extraction and Analysis", (Embedded Tutorial), Proceedings from the 12th International Conference on VLSI Design, Jan 7 – 10 1999
- Timothy Kam, Sishpal Rawat, Desmond Kirkpatrick, Rabindra (Rob) Roy, Gregory S. Spirakis, Naveed Sherwani, and Craig Peterson; "EDA Challenges Facing Future Microprocesor Design", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 19, No. 12, December 2000, Pgs. 1498 – 1506
- Don MacMillen, Michael Butts, Raul Camposano, Dwight Hill and Thomas W. Williams, "An Industrial View of Electronic Design Automation", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 19, No. 12, December 2000, Pgs. 1428 – 1448
- Linda Geppert, "Electronic Design Automation", IEEE Spectrum, January 2000, Pgs. 70 – 74

- Mohammad Hossein Reshadi, Amir Masoud Gharehbagi and Zainalabedin Navabi; "AIRE/CE: A Revison Towards CAD Tools Integration", 12th International Conf. On Microelectronics, Oct. 31 – Nov. 2 2000, pgs 277 – 280
- U.S. Patent No. 6,728,590 to Dean
- U.S. Patent No. 6,581,191 to Schubert et al.
- U.S. Patent No. 5,855,009 to Garcia et al.
- U.S. Patent No. 6,115,546 to Chevallier et al.
- U.S. Patent No. 6,618,839 to Beardslee et al.
- U.S. Patent No. 6,513,024 to Li
- U.S. Patent No. 6,662,323 to Ashar et al.
- U.S. Patent No. 6,343,370 to Taoka et al.
- U.S. Patent No. 6,216,652 to Dangelo
- U.S. Patent No. 5,801,958 to Dangelo
- U.S. Patent No. 6,446,243 to Huang et al
- U.S. Patent No. 6,591,402 to Chandra et al.
- U.S. Patent No. 6,397,373 to Tseng et al.
- U.S. Patent No. 5,812,416 to Gupte et al.

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Morella Rosales-Hanner whose telephone number is (703) 305-8883. The examiner can normally be reached Monday-Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703 308-6647. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH

Aug. 20th, 2004

JEAN R. HOMERE
PRIMARY EXAMINER